



***New features in SMASH™ 5.5.0***

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## THANKS

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to [smash@dolphin-integration.com](mailto:smash@dolphin-integration.com) with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be sure we will try to take it into account in a future release.

## INTRODUCTION

The focus of the SMASH 5 releases is on the adaptation for hierarchical design of Systems-on-Chip and mixed signal virtual Test-Bench.

This includes:

- Multi-level zooming and bifocalization to define a grade of equivalence while comparing two levels (i.e. for proving that any higher model level is a truthful, albeit less accurate substitute to a lower level)
- The increase of designers' productivity: speed of set-up, user interface, relevance of debug functions, separation of the test bench and the circuit...
- Interfacing for complementing the simulation Engine (kernel):
  - For productivity enhancing with schematic captures...
  - For Virtual Test with Raisonance, Keil, Matlab/Simulink, National Instruments...

SMASH 5 will provide all the designers with explosive improvements of mixity between languages and description levels with a single engine. The table below highlights:

- (1) the capability to instantiate "a language"
- (2) into a model of "another language"

|     |                    | (1)                      |                  |                  |                  |                |                    |
|-----|--------------------|--------------------------|------------------|------------------|------------------|----------------|--------------------|
|     |                    | <i>C</i>                 | <i>SPICE</i>     | <i>VHDL</i>      | <i>VHDL-AMS</i>  | <i>Verilog</i> | <i>Verilog-AMS</i> |
| (2) | <i>SPICE</i>       | ABCD/AMD                 | ✓                | ✓                | ✓                | ✓              | ✓                  |
|     | <i>VHDL</i>        |                          | 5.x <sup>1</sup> | ✓                | ✓                | ✓ <sup>3</sup> | 5.x <sup>1</sup>   |
|     | <i>VHDL-AMS</i>    |                          | 5.x <sup>1</sup> | ✓                | ✓                | ✓ <sup>3</sup> | 5.x <sup>1</sup>   |
|     | <i>Verilog</i>     | DMD/SystemC <sup>2</sup> | ✓                | ✓ <sup>3</sup>   | ✓                | ✓ <sup>4</sup> | ✓                  |
|     | <i>Verilog-AMS</i> |                          | ✓                | 5.x <sup>1</sup> | 5.x <sup>1</sup> | ✓              | ✓ <sup>5</sup>     |

<sup>1</sup> Mixity improvements scheduled in the roadmap of SMASH 5.x.

<sup>2</sup> Not yet supported in SMASH 5.5.0. Support scheduled in SMASH 5.5.x update.

<sup>3</sup> Currently limited to scalar STD\_LOGIC signals.

<sup>4</sup> Partial Verilog-95 support including some Verilog-2001 features. Full Verilog-95 & Verilog-2001 in the roadmap of SMASH 5.x.

<sup>5</sup> Partial Verilog-A support for microelectronics designs. Full Verilog-A & Verilog-AMS extensions in the roadmap of SMASH 5.x.

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## VERILOG-A

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Verilog-AMS benefits designers by allowing them to describe and simulate analog and mixed signal designs using a top-down design methodology as well as the traditional bottom up approach. Moreover, Verilog-AMS provides powerful structural and behavioral modeling capabilities for systems in which the effects of, and interactions among, different disciplines like electrical, mechanical and thermal are important.

**SMASH 5.5 extends its natively mixed-language and mixed-signal single kernel to Verilog-A with seamless hierarchical mixing with SPICE.**

In addition to already supported description languages, a Verilog-A subset targeting micro-electronic designs is now supported by SMASH. This subset supports mixed-signal multi language transient analysis of conservative and signal flow systems with:

- Natures, disciplines and nets
- Analog signals and contribution statements
- Time derivative and integral analog operators
- @cross monitored event
- Environment parameter functions
- Standard definitions of disciplines & constants

Furthermore, SMASH provides natural use of library statements (.LIB) for specification of Verilog and Verilog-A libraries of modules. Dependency handling is completely automatic, thereby freeing the designer from manual recompilation of modified descriptions. Furthermore, the compiled “black-box” modules can be used directly and even delivered pre-compiled, for instance for evaluation purposes, thereby providing IP protection.

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## VERILOG-HDL

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The Verilog-95 parser of previous releases of SMASH has been replaced by a full Verilog-HDL compliant parser supporting Verilog-95, Verilog-2001 & Verilog-AMS. The new parser provides more standards compliant parsing and paves the way to Verilog-2001 and SystemVerilog.

**SMASH 5.5 delivers a new Verilog-HDL elaboration and simulation infrastructure built on the new parser.**

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## SDF

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The new Verilog-HDL parser does not support the non standard SDF parsing of previous SMASH releases. An upcoming update of SMASH 5.5 will deliver a fully SDF standard compliant VPI module integrated in the new Verilog-HDL parsing, elaboration and simulation infrastructure.

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## DMD

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DMD modules for logic C descriptions are not yet reintegrated. An upcoming update of SMASH 5.5 will provide DMD modules integrated in the new Verilog-HDL elaboration and simulation infrastructure.

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## SWIFT - ACCELERATION USING DEVICE MODEL APPROXIMATION

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The SWIFT device model approximation uses a combination of a simplified device model (light evaluation) and a full device model (accurate evaluation) to accelerate transient analysis of transistors. The simplified model mode corresponds to a linear approximation of conductance and associated currents. This fast evaluation is applied when the change of all node voltages is under a criterion defined by the user. A mixed mode, combination of the simplified device model and the full device model, is applied when switching from fast evaluation mode to accurate evaluation mode in order to ensure continuity between the two modes. This mixed mode corresponds to a polynomial curve of conductance and associated currents.

As implemented in this release of SMASH™, the user only needs to specify the value which defines the threshold between the approximation and the non approximation modes. This algorithm makes no simplifying hypothesis on weak couplings between nodes. Furthermore, it has the advantage of having a reduced loss of accuracy while providing fast simulation. The resulting simulation is 2 to 3 times faster for a loss of accuracy of less than 1%.

**Note:**

*A dedicated application note is available upon request.*

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## SUPPORTED PLATFORMS

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### Microsoft Windows

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SMASH™ is designed to run under Microsoft Windows NT/2000/XP.

### Sun Solaris on SPARC platform

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SMASH™ is designed to run under Sun Solaris 7 and 8 on the SPARC platform.

### Linux on Intel x86 platform

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SMASH™ is designed to run under the Linux distributions on the i86 platform detailed in the following table. SuSE Linux 8.0, Red Hat Linux 7.3, 8.0 and 9.0, as well as Red Hat Enterprise Linux 3.0.

| MainWin | Linux                                   | GNU C Library        | XFree |
|---------|---|----------------------|-------|
| 5.0.3   | RedHat Linux 7.3                        | 2.2.5-34             | 4.3   |
|         | RedHat Linux 8.0                        | 2.2.93-5             |       |
|         | RedHat Linux 9.0                        | 2.3.2-27.9 or higher |       |
|         | RedHat Enterprise Linux 3 (ES, AS & WS) | 2.3.2-95.3 or higher |       |
|         | SuSE Linux Enterprise Server 8          | 2.2.5-164            |       |
|         | SuSE Linux Enterprise Server 9          | 2.3.3-98.28          |       |

- SMASH™ is developed and validated mainly on Red Hat Linux. However, customers deploy on various Linux distributions without any issues.
- The supported GNU C library (glibc) versions for Red Hat Linux 7.3 and 8.0 are the default versions, which come with the Red Hat Linux distribution. The default version that comes with Red Hat Linux 9 is usually glibc-2.3.2-11.9, which still has some bugs that may prevent SMASH™ from running correctly.

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## WEB SITE

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Our web site <http://www.dolphin-integration.com/> is a possible source of information (and promotional offers from time to time). Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

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## ADDRESSES

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Customers regularly ask where for the following addresses:

### Where to find the IEEE standards

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Institute of Electrical and Electronics Engineers, Inc.  
445 Hoes Lane, P.P. Box 1331, Piscataway, NJ 08855-1331, USA  
<http://www.ieee.org/>  
<http://www.standards.ieee.org/>

**IEEE 1364-1995, Verilog Hardware Description Language Reference Manual**

**IEEE Std 1076-1993, VHDL**  
<http://www.vhdl.org/>

### Where to find EDA on the web

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<http://www.eda.org/>  
<http://www.accellera.org/>  
<http://www.parmita.com/verilogfaq/>  
<http://www.verilog.com/>  
<http://www.deeps.org/verilog/index.html>

### Where to SPICE models on the web

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<http://www-device.eecs.berkeley.edu/~bsim3/>  
<http://www-device.eecs.berkeley.edu/~bsimsoi/>  
<http://legwww.epfl.ch/ekv/>  
[http://www.semiconductors.philips.com/Philips\\_Models/index.html](http://www.semiconductors.philips.com/Philips_Models/index.html)  
<http://www2.fht-esslingen.de/institute/iafgp/neu/VBIC/index.html>

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## CREDITS & COPYRIGHTS

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### Gear-Brayton Integration Method

The new formulation of the Gear-Brayton integration method included in SMASH was perfected and implemented at Supélec - Service des Mesures.

### Scintilla Source Code Editor Component

License for Scintilla and SciTE  
Copyright 1998-2005 by Neil Hodgson <[neilh@scintilla.org](mailto:neilh@scintilla.org)>  
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### wxWidgets: A free C++ framework for cross-platform programming

<http://www.wxwidgets.org/>

wxWindows Library License, Version 3  
Copyright (C) 1998 Julian Smart, Robert Roebing [, ...]

WXWINDOWS LIBRARY LICENCE

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## VIEWER

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### Enhancements

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- Implemented progress bar display in status bar during simulation (SMASH 5.4.2).
- Implemented 64 bit compatible file seek operations to correctly handle file sizes greater than 2GB, in particular for waveform files (SMASH 5.4.2).
- Enable printing of waveforms during simulation (SMASH 5.4.2).
- Implemented an option for not saving data at each break point to reduce the size of waveform files in the case of mixed-signal simulations (DDIsa02528 – SMASH 5.4.2).
- Implemented option to display print markers for waveform differentiation when copying waveform windows (DDIsa02452 – SMASH 5.4.2).

### Modifications

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- Enable "*Run operating point analysis for initial state*" when no stable state has yet been obtained (DDIsa02499 – SMASH 5.4.2).
- Improved graphic handling of cosmetics, in particular moving and deleting of cosmetic (DDIsa01142 – SMASH 5.4.2).

### Bug fixing

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- Corrected run button of Sweep dialog box which was not always starting the simulation when selected (DDIsa02458 – SMASH 5.4.2).
- Corrected FFT dialog when run from generic window which was crashing when invalid values were entered (DDIsa02548 – SMASH 5.4.2).

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## BATCH

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### Enhancements

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- Implemented Command Line Interface (CLI) to Verilog & Verilog-AMS compiler for future batch scripts and batch compilation of descriptions (SMASH 5.5.0).

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## KERNEL

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### Enhancements

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- Improved creation of archive when using .ARCHIVE directive which now creates a standard zip archive (SMASH 5.4.2).
- Implemented 64 bit compatible file seek operations to correctly handle file sizes greater than 2GB, in particular for waveform files (SMASH 5.4.2).

- Implemented an option for not saving data at each break point to reduce the size of waveform files in the case of mixed-signal simulations (DDIsa02528 – SMASH 5.4.2).
- Allow the use of parameter name 'VER' as an alias of 'VERSION' in model parameter sets (DDIsa02555 – SMASH 5.4.2).
- Implemented automatic dependency handling and library (.LIB) recompilation as needed when loading or reloading a circuit. It should no longer be necessary to perform an unneeded modification to the netlist or pattern file in order to force a reload of the circuit when underlying include or library files have changed (SMASH 5.5.0).

### **Modifications**

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- Improved handling of reported error when loading library which did not interrupt circuit loading (DDIsa02505 – SMASH 5.4.2).
- Implemented workaround for elaboration order issue in formulas of device values (DDIsa02449 – SMASH 5.4.2).
- Implemented device specific INOISE and ONOISE display with noise type (flicker, thermal or shot) (DDIsa01282, DDIsa02249 – SMASH 5.4.2).
- Depending on the SPICE flavor, use either 'LN' or 'LOG10' functions for implementing the 'LOG' function in formulas (DDIsa02562 – SMASH 5.4.2).

### **Bug fixing**

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- Corrected the reported transistor states in the operating point file when running a power-up analysis (DDIsa02542 – SMASH 5.4.2).
- Corrected SPI3 waveform file reading to accept ELDO generated files (DDIsa02271 – SMASH 5.4.2).
- Corrected instantiation of SMASH specific mixed-language SPICE sub-circuits from Verilog which was not correctly instantiating the SPICE fork of the mixed-language sub-circuit (DDIsa01750 – SMASH 5.4.2).

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## **SPICE**

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### **Enhancements**

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- Implemented device specific INOISE and ONOISE display with noise type (flicker, thermal or shot) (DDIsa01282, DDIsa02249 – SMASH 5.4.2).
- Allow the use of parameter name VER as an alias of VERSION in model parameter sets (DDIsa02555 – SMASH 5.4.2).

### **Modifications**

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- Implemented workaround for elaboration order issue in formulas of device values (DDIsa02449 – SMASH 5.4.2).
- Depending on the SPICE flavor, use either LN or LOG10 functions for implementing the LOG function in formulas (DDIsa02562 – SMASH 5.4.2).

### **Bug fixing**

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- Corrected the minimum and maximum value of the integrated noise (DDIsa02527 – SMASH 5.4.2).
- Corrected the reported transistor states in the operating point file when running a power-up analysis (DDIsa02542 – SMASH 5.4.2).

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## VERILOG & VERILOG-AMS

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### Enhancements

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- Integrated a Verilog-95, 2001 & AMS compliant parser with Verilog-2001 compatible preprocessing (SMASH 5.5.0).
- Implemented Verilog-A subset for micro-electronic designs (SMASH 5.5.0).
- Verilog & Verilog-AMS descriptions can be compiled for IP protection allowing black-box delivery of precompiled models (SMASH 5.5.0).
- Implemented automatic dependency handling and library (.LIB) recompilation as needed when loading or reloading a circuit. It should no longer be necessary to perform an unneeded modification to the netlist or pattern file in order to force a reload of the circuit when underlying include or library files have changed (SMASH 5.5.0).
- Implemented tracing of Verilog reg variables in addition to signals (DDIsa01066 – SMASH 5.5.0).
- Implemented Command Line Interface (CLI) to Verilog & Verilog-AMS compiler for future batch scripts and batch compilation of descriptions (SMASH 5.5.0).
- Implemented `$display` support of `%d` format specification with more the 32 bits variables (DDIsa01857 – SMASH 5.5.0).
- Implemented `force` and `release` procedural continuous assignment statements except in `fork` parallel blocks (DDIsa00526 – SMASH 5.5.0).
- Implemented `posedge` and `negedge` for event control with vector expressions (DDIsa01955 – SMASH 5.5.0).
- Implemented abort of simulation for `$stop` system task (DDIsa01944 – SMASH 5.5.0).
- Implemented procedural assignment of of reg with more than 32 bits to real variable (DDIsa01287 – SMASH 5.5.0).
- Take `.SELECTDELAY` directive into account at simulation phase instead of at code generation phase (DDIsa01997 – SMASH 5.5.0).
- Implemented extraction of function argument in sensitivity list of continuous assignment (DDIsa01758 – SMASH 5.5.0).

### Modifications

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- SDF annotation is not yet supported on the new parsing, elaboration and simulation infrastructure (SMASH 5.5.0).
- Apply gate delays at operating point (DDIsa01762 – SMASH 5.5.0).

### Bug fixing

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- Corrected procedural assignment of real values to reg variables (DDIsa01846 - SMASH 5.5.0).

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## VHDL & VHDL-AMS

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### Enhancements

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- Changed empty file warning to failure in order to avoid infinite recursion during dependency handling and unit obsolescence checks (DDIsa00460 – SMASH 5.4.2).

### Bug fixing

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- Corrected the `WRITE(TIME)` display format according to the specified unit (DDIsa02519 – SMASH 5.4.2).

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## MODELS (C, D, E, F, G, H, I, J, K, L, M, Q, R, V)

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### Enhancements

---

- Implemented device specific INOISE and ONOISE display with noise type (flicker, thermal or shot) (DDIsa01282, DDIsa02249 – SMASH 5.4.2).
- Allow the use of parameter name VER as an alias of VERSION in model parameter sets (DDIsa02555 – SMASH 5.4.2).

### Bug fixing

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- PULSE: corrected the default values of sources when corresponding parameters are not specified (DDIsa02169 – SMASH 5.4.2).
- BSIM3v3 & Level49: corrected the overlap capacitances expression of PMOS which was not correct for certain specific parameter sets (DDIsa02533 – SMASH 5.4.2).
- COUPLING: corrected the coil current expression for taking in count the coupling effect (DDIsa02541 – SMASH 5.4.2).
- Corrected the reported transistor states in the operating point file when running a power-up analysis (DDIsa02542 – SMASH 5.4.2).

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## TRANS

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### Enhancements

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- Implemented device specific INOISE and ONOISE display with noise type (flicker, thermal or shot) (DDIsa01282, DDIsa02249 – SMASH 5.4.2).

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## SHAKER

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### Modifications

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- Continue extraction even if nothing is given after the `.COMMAND` (DDIsa02342 – SMASH 5.4.2).

