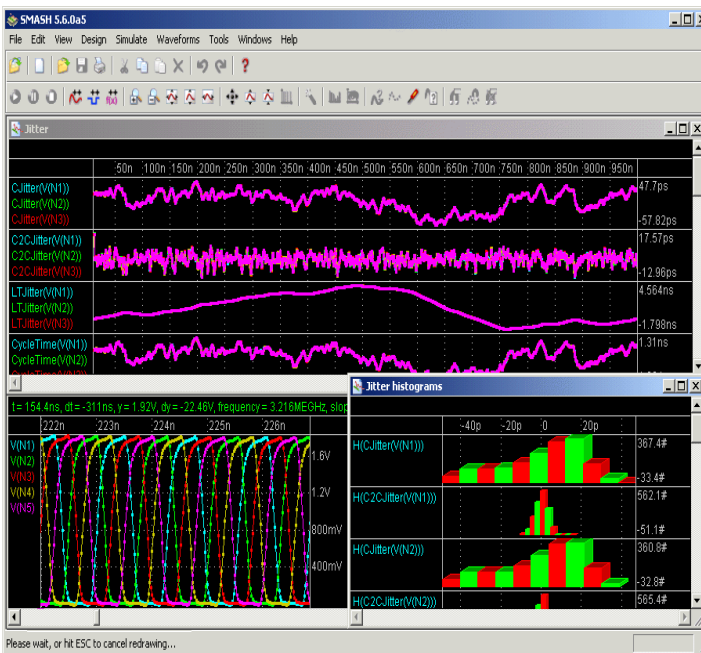


Due to the ever-lasting need for performance improvements, mixed signal designers face the challenge of simulating ever more accurately the effect of jitters in embedded Virtual Components (ViC) such as PLLs or DLLs. Unpredictable Jitters degrade systematically the expected performances of the whole System-on-Chip and, even worse, may induce drastic losses of design yield, down to making a System-on-Chip totally non-functional, unless you can benefit from SMASH 5.6.



## KEY FEATURES

Measuring on transient logic or analog waveforms:

- Cycle jitter versus time
- Cycle-to-cycle jitter versus time
- Long term jitter versus time
- Cycle time versus time
- Frequency versus time
- Histogram and dispersion of cycle jitter
- Histogram and dispersion of cycle-to-cycle jitter
- Histogram and dispersion of long term jitter

## JITTER MEASUREMENTS

Jitter evaluation still is a mystic problem in search of efficient solutions. However, our Jitter analysis protocol provides means for simulating the intrinsic jitters (cycle jitter, cycle-to-cycle jitter and long term jitter) and for comparing it with objectives so as to perform its acceptance.

Thanks to the transient noise simulation, all kinds of jitter now can be simulated:

- intrinsic jitter due to the noise of components (transistor, resistor...)
- structural jitter due to the architecture of the design.
- cycle jitter, cycle-to-cycle jitter and long-term jitter is computed from transient simulation result.

Simulating the jitters themselves, as well as the impact of jitters on designs, is turned into a quick and fun task with SMASH 5.6.



**SMASH is available identically under Linux, Solaris and Windows.**