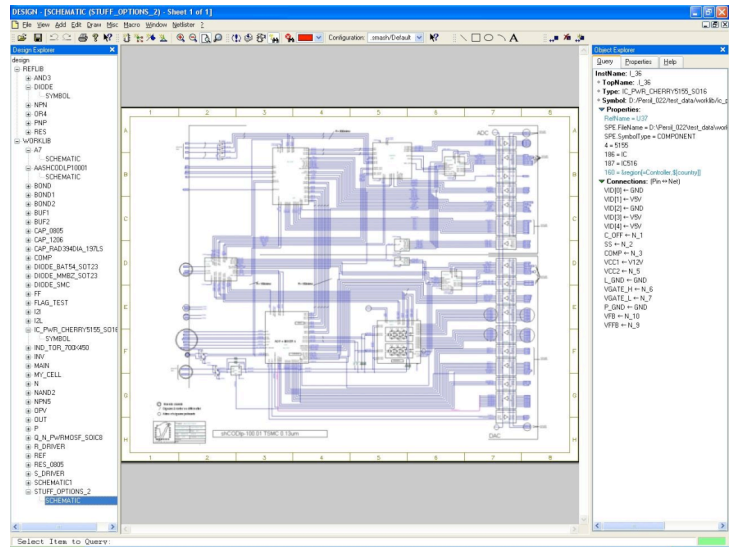


SLED is a hierarchical schematic entry solution of the **third generation** which delivers the long awaited dual capability for Graphic Entry and Scriptability at once. It blends efficiently the feasibility of linking components and of writing scripts for configuring a netlist hierarchically. Interoperability with other schematic entry tools is ensured for capitalizing on legacy designs and cooperative work, and interoperability in the Design Chains is ensured through standard design exchange formats and scriptability for customization by CAD managers.

### KEY FEATURES

- ✓ Hierarchical schematic entry
- ✓ Schematic structure navigator with hierarchical net highlighting and back-annotation display
- ✓ Design library browser with dynamic access to project work libraries & Design Kit reference libraries
- ✓ **SledNet** for Mixed-signal and multi-lingual netlisting in SPICE, Verilog-HDL & VHDL
- ✓ Scripting capabilities with database access for ERC checks... both batch and interactive
- ✓ Import of designs from legacy ECS entry solutions including Synario, Cohesion HDS & Laker-AMS
- ✓ Multi-platform for productivity in heterogeneous networks



### PRODUCT CHARACTERISTICS

The capability for mapping HDL code of any Hardware Description Language graphically throughout the design hierarchy has been reassessed to facilitate the creation, orderly assembly, verification and reuse of models for synthesis or simulation.

SLED allows multiple levels of descriptions for system or single block validation, while combining SPICE and HDL representations, to ease architectural design of any System-On-Chip. A system can be iteratively validated by using a SPICE representation of a single block, while all other blocks in the system are represented in HDL for a full functional mixed signal simulation. It is fundamental for state-of-the-art hierarchical designs of multi-domain components.

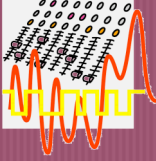
Endowed with a full library of input sources and active text for simulation directives, SLED combines with SMASH to allow the documentation of a full testbench for optimization of concurrent design. It serves to set-up the "Design of Experiments" as well as sign-off documentation. Virtual Testbench representations facilitate project management and hence shorten design cycles.



**SLED is available identically under Linux, Solaris and Windows.**



### MEDAL



Compared to some integrated solution, **SLED is both framework independent and open to bridging** with EDA tools for interoperability at different levels of the Design Chains.

A sketch on generations: on request.

#### ✓ Easy access to netlists

Multilingual and hierarchical Netlists are generated in de-facto or IEEE standard languages such as SPICE, Verilog-HDL and VHDL, and are easily accessible for linking with other tools in the Design Chain, such as Layout versus Schematic (LVS).

#### ✓ Import of whole libraries and designs

From any release of the legacy ECS™ stem including Synario™, Cohesion Systems™, Laker AMS™...

#### ✓ ASCII storage format

Storage of design data, including design or reference library configuration files, symbols, schematics... in ASCII format enables generation using a script based approach for automatic symbol generation, library conversion, design library setup...

#### ✓ EDIF Import/Export

Import/Export to and from EDIF provides the means to exchange full schematics, including graphics, with other design entry solutions, as well as to transfer designs to the next step in your Design Chain, such as Schematic Driven Layout (SDL).

#### ✓ Open to any Revision Control System

The use of ASCII based files, instead of binary files, for storing design data, and the possibility to trigger actions in the design environment allows complete integration with the Revision Control System of your choice.



#### ✓ Schematic consistency checks

Save time thanks to early error detection during design with coherency checks, i.e. symbol vs. model I/O, and online Electrical Rule Checks (ERC), i.e. shorted output pins...

Such checks can also be enriched through the scripting capabilities.

#### ✓ Batch netlisting

For direct integration into test harnesses and automated design regression testing, batch netlisting allows to generate netlists without opening the graphic environment.

#### ✓ Batch scripting interface

A scripting API (Application Programming Interface) enables direct database access for custom scripts allowing batch schematic generation, manipulation and verification.

#### ✓ Design of Experiments (DoE)

Paving the way to DoE, a library of input sources provides the building blocks for complete graphic testbench design.

## MEDAL Presentation Sheet



**SLED is available identically under Linux, Solaris and Windows.**