

SMASH as Missing **EDA Link**

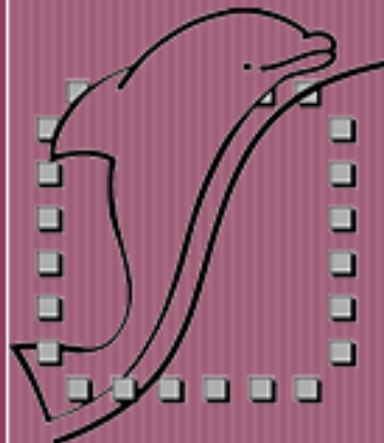
Single kernel
Mixed-signal
Multi-language
Multi-level

DOLPHIN INTEGRATION

The Enabler of Mixed Signal Systems-on-Chip

SMASH is one of the Missing EDA Links from the Dolphin Integration offering. It is the perfect simulation solution for the **development and verification of logic and mixed-signal Virtual Components (ViC) and Systems-on-Chip (SoC)** as it brings added value to standard design flows, as a point product, and completes custom design flows.

One of the main focuses of SMASH is to deliver innovative features that enable **efficient detection of design defects** while **tuning the speed accuracy tradeoff** using appropriate multi-level modeling of the different parts of the circuit.





Logic & Mixed signal simulation made easy

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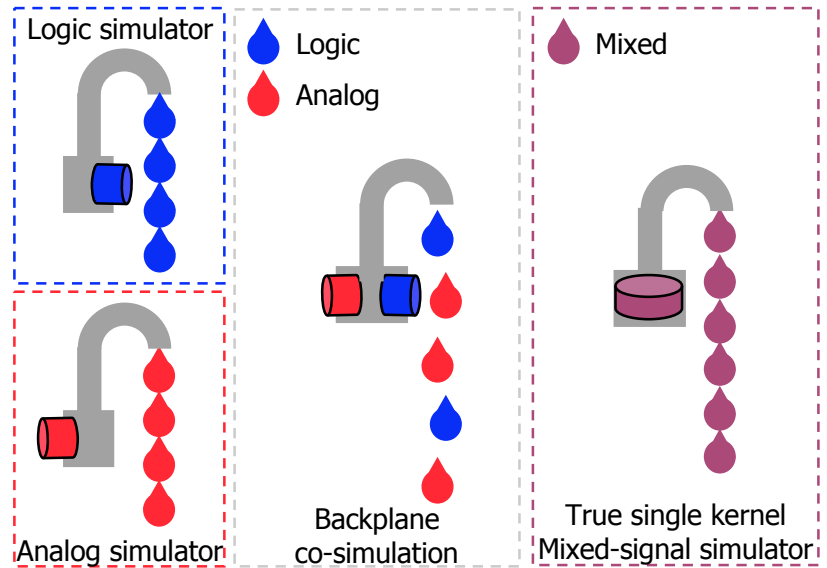
SMASH versus traditional signal mixers

The signal flows handled by electronic simulators require efficient mixing to enable tapping data from diverse sources. The simplest image is that of faucets delivering hot and cold water representing analog and logic signals, but the concept is more general as other sources must be dealt with, like spectral or digital sources...

Beyond the dual knob mixer tap, SMASH provides the performance of a single-lever mixer faucet with no compromise on accuracy!

KEY FEATURES

- ✓ Hassle-free mixing from diverse sources
- ✓ SoC as Virtual PCB: no backplane injecting delays and disturbances
- ✓ Single kernel for best leverage of accuracy and speed
- ✓ Specific algorithms for fast detection of design bugs
- ✓ Mixed signal for accurate and reliable simulations
- ✓ Multi-lingual for mixed-language sources
- ✓ Multi-level for hierarchical design with inter-level calibration



Entering a mixed signal design tends to be done through a mixed signal HDL-AMS language, generally more abstract than schematic entry. Until now, the difference between analog and logic schematics was the amusing absence of power supply lines in the latter. It no longer can be treated as an innocent simplification as power lines must be taken into account either for self-control of voltage supply levels by circuitry itself, or for inserting checkers of consistency of power management.

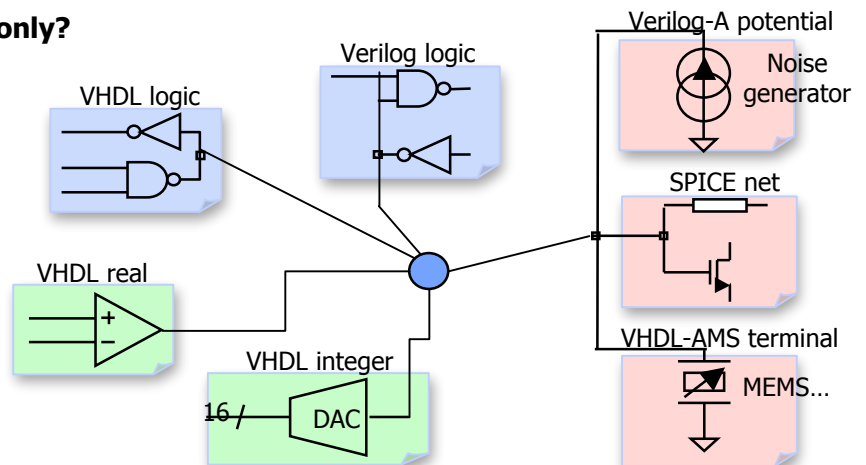
While Schematics editors facilitate top-down and bottom-up navigation for hierarchical design flows, traditional simulators end up restricting flexibility of modeling to referring to pure SPICE, lest the co-simulation would be too complex or, even worse, not reliable at all.

Why have two knobs and enable hot water only?

INTERFACE DEVICE CAPABILITIES

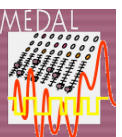
A unique interface device enables simultaneous interconnection of analog nets and logic signals of different natures, with automatic parameterized conversions, allowing mixing of:

- ✓ Multiple languages (VHDL, Verilog, SPICE, Verilog-A, VHDL-AMS)
- ✓ Multiple net and signal types (std_logic, real, integer, terminal, potential...)



  **SMASH is available identically under Linux and Windows.**

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A multiple language support All-in-One simulator

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Analog, Logic & Mixed-Signal Simulator

Integrating Systems-on-Chip must not demand the remodeling of virtual components, when embedding them, for making them fit the limitations of a specific simulator. Furthermore, efficient SoC Integration requires allowing simultaneous **bottom-up and top-down design** while enabling the designer's choice of the appropriate abstraction levels to enable complete multi-level simulation for full-chip verification of mixed SoC.

SMASH promotes simulation as natural as analog & mixed-signal schematics entry, using a natively mixed-signal multi-language circuit description, be it HDL text or netlist!

KEY BENEFITS

- ✓ Natural "All-in-One" approach of analog, logic & mixed-signal multi language simulation (SPICE, Verilog HDL, Verilog-A, VHDL, VHDL-AMS, ABCD, SystemC, C...)
- ✓ No backplane, no distortions, no delays!
- ✓ Easy combination of standard design languages at any abstraction level (electrical, structural, synthesizable RTL, behavioral, or architectural levels)
- ✓ Straightforward cross-language model instantiation using common language statements (SPICE/X...)
- ✓ Optimization of speed vs. accuracy trade-offs using models of the appropriate abstraction levels
- ✓ Flexible support of SPICE flavors (Hspice, Pspice, Eldo...) for easy integration into Design Chains
- ✓ Top-notch support of VHDL-AMS for multi-domain modeling and simulation

SMASH "All-in-One" simulator enables the ultimate ascertainment of Multi-level Equivalence in simulations, both top-down and bottom-up, inclusive of Silicon Qualification.

SMASH: Logic & Mixed Signal simulation made easy!

All in One Logic & Mixed Signal Simulator

- ✓ Ease of Use
- ✓ Speed & Accuracy
- ✓ Efficient debugging features
- ✓ Already thousands of users

The Enabler of mixed signal Systems-on-Chip

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MEDAL

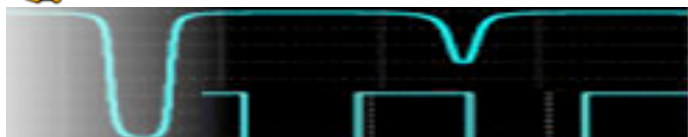
Toward Assertion-Based Verification with PSL Support

Relevant options of SMASH include native support for simulation of **PSL** (Property Specification Language) properties, both **assertions** and **coverage**, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.



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A solution for Application Function simulations

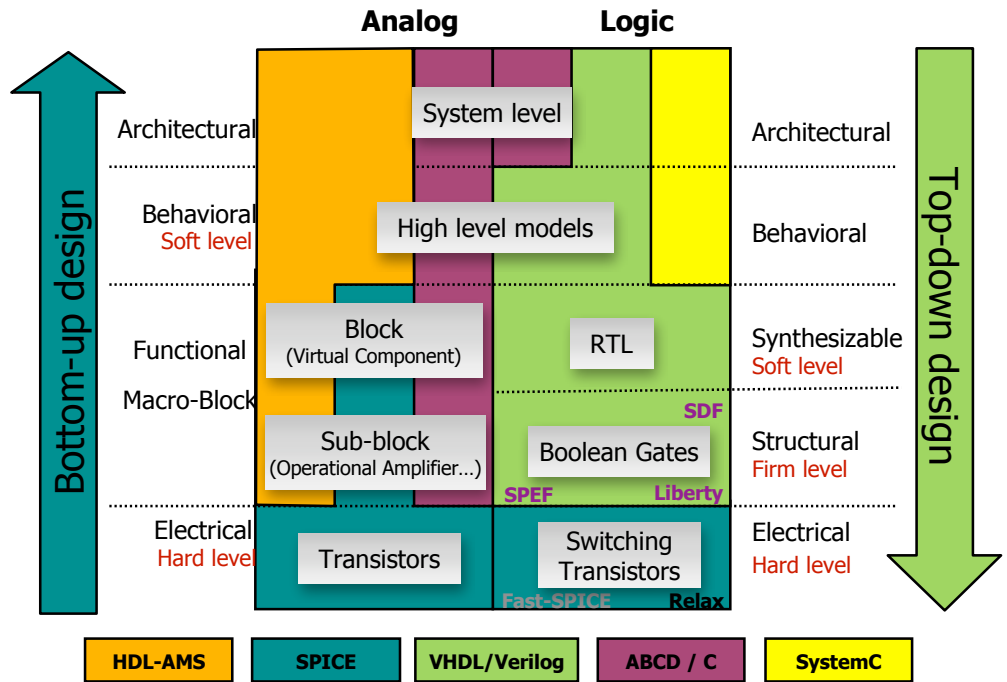
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Two-sided tower of levels for multi-level zooming

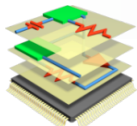
To promote mixed-signal simulation and explain multi-level concerns, a representation as the "Tower of levels" is particularly effective with its two sides, analog and logic. Multi-level zooming and equivalence checking is a critical capability for designers to reduce their development time by increasing the simulation speed and relevance at once.

KEY BENEFITS

- ✓ Only one simulation to simulate functions mixing several levels (Analog in Spice at electrical level, Logic in Verilog at structural level, and a large analog function in behavioral)
- ✓ Efficient Speed vs. Accuracy trade-off thanks to the mixing of levels
- ✓ Simulation time saving and faster bug identification
- ✓ No need to modify the netlist since all languages are directly supported



Multi-level simulation has never been so easy!



For a complete front-end offering



SLED, the Schematic Link Editor

SLED is a hierarchical schematic entry solution of the third generation allowing designers to perform graphic entry and configuration of their designs in a shorter time. For a real compatibility with SMASH, it enables the creation of true mixed-signal circuits, multi-level and multi-domain systems.

- ✓ User friendly interface with high efforts made on ease of use
- ✓ Multiple level of descriptions for system or single block validation to ease architectural design of SoC
- ✓ Improved productivity with the "Devices" library including basic logic and analog components
- ✓ Quick localization of design problems through user configurable Design Rule Checker
- ✓ Dynamic link with SMASH for schematic driven design

SCROOGE TLA, the power consumption estimator

SCROOGE TLA, powered by SMASH, grants logic, analog and mixed-signal designers with the capability to quantify power consumption, to track and to detect power peaks or hot points.

It is the ideal solution even for users with layout, P&R or power analyzer solutions, as it can predict performance accurately on the basis of synthesis only.

- ✓ Capability to analyze hierarchically mixed-signal sensitivity to power consumption
- ✓ Extraction of power consumption values (DCDC current, charge deficit, output capacitance) allowing to select and size DC-DC switching regulators
- ✓ Possibility to customize html reports for best relevance in design reviews
- ✓ Interactive validation and optimization of the power budget

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