

Dolphin presents a state-of-the-art methodology for a fast and accurate specification of Jitter in a SoC by simulation to identify the Jitter Budget, benefiting from a patent on offset in SMASH. Three categories of configurations can be encountered with synchronization problems: Multiprocessors and Memories, Digital Transmission Processors, Analog Communication (Codecs).

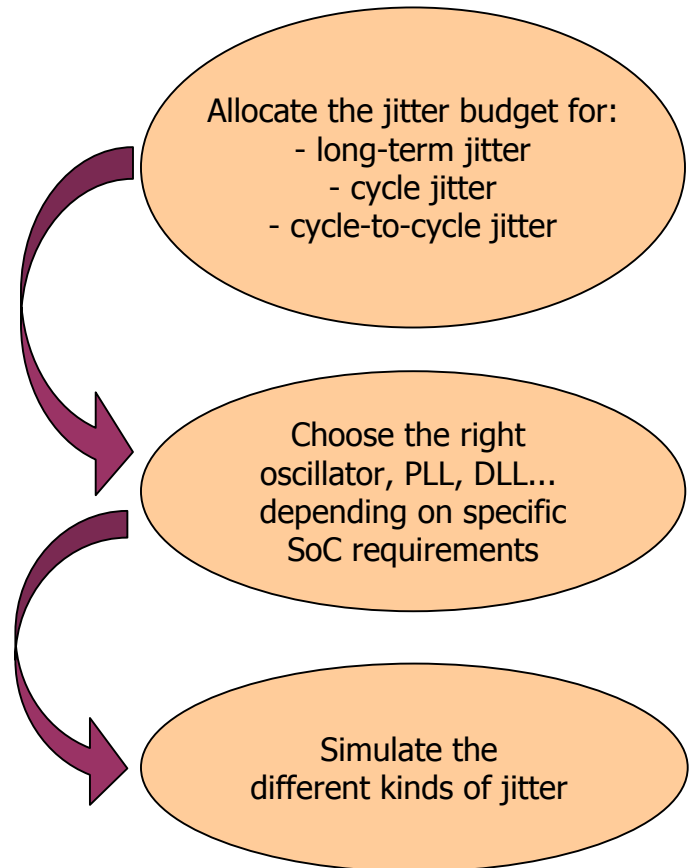
Protocol Overview

Simulation stage showing the specific influence of:

- Long-term Jitter
- Cycle Jitter
- Cycle-to-cycle jitter

*Application Note
available on request*

Methodology to simulate all kind of jitters:
This stage is based on transient-noise analysis as available in a mixed signal simulator like SMASH.



OVERALL JITTER MASTERY

Jitter specification and simulation is still perceived as a magic problem for which no efficient solution could be found.

With core competencies as both a Virtual Component provider and an EDA tool provider with mixed signal expertise, Dolphin Integration can propose a complete methodology for:

- (1) the SoC Integrator to defining the appropriate Jitter depending on the SoC requirements (see above).
- (2) the PLL designer to ascertain that he meets the Jitter Budget itself.

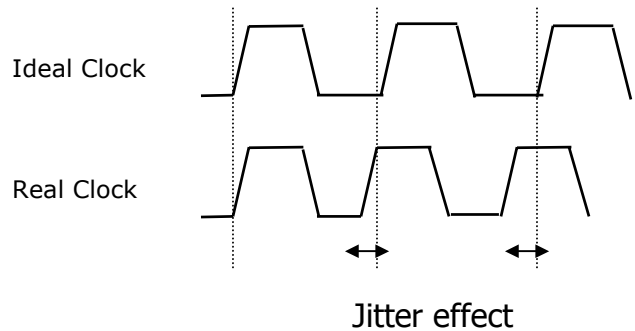
This overview complements the unique simulation capabilities of SMASH with all the guidance of appropriate “operating protocols”.



Due to the ever-lasting need for performance improvements, mixed signal designers face the on-face the on-going challenge of simulating ever more accurately the jitter effect in embedded embedded Virtual Components (ViC) such as PLLs or DLLs. Unpredictable Jitter degrades degrades systematically the expected performances and, even worse, may induce drastic design drastic design yield losses down to making a System-on-Chip totally non-functional.

Key features

- Transient noise simulation
- Multi-level modeling
- Noise sources development



THE DOLPHIN METHOD

Jitter evaluation is still a mystic problem for which no efficient solutions have been found. However, depending on the simulation capabilities of SMASH, our Jitter analysis analysis protocol provides the means for designers to measure the intrinsic jitter and to and to compare it with the objective to conclude on its acceptability

Jitter could be simulated using a transient noise method: such a method however is applicable only to circuits with a small number of transistors, as it is too time and memory memory consuming.

The Dolphin analysis protocol drastically shortens simulation time for diagnosing jitter. In jitter. In addition to embedding specific algorithms for computing the noise contribution of contribution of each component during a transient simulation, SMASH is a mixed signal signal and multi level simulator as required by this method:

- to slice the circuit and to apply a transient noise simulation to each sub-block in order to order to characterize their noise model avoiding a too long SPICE simulation of the complete circuit.

-to describe each sub-block in continuous time-series such as the AMS model of the filter, the filter, the VCO, and the charge pump for a PLL. Multi-level design enables a behavioral behavioral transient simulation including the noise effect results extracted from the previous step.

Note for fabrication process variants: SMASH additionally allows flexible development development and management of new noise models. The integration of noise sources is sources is facilitated by the TRANS development Kit for device models.

promotion sheet

